AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of the claims:

1. (Withdrawn) A method of fabricating a memory, comprising steps of:

forming a storage material film on a first electrode film;

forming a storage part and an etched thin-film part by partially etching said storage material film by a prescribed thickness;

forming an insulator film to cover at least said thin-film part of said storage material film; and

patterning said insulator film and said thin-film part of said storage material film by forming an etching mask on a prescribed region of said insulator film and thereafter etching said insulator film and said thin-film part of said storage material film through said etching mask.

2. (Withdrawn) The method of fabricating a memory according to claim 1, wherein

said step of forming said storage part and said thin-film part includes a step of partially etching said storage material film so that said thin-film part has a thickness of at least about 15% of the thickness of said storage material film on the average.

3. (Withdrawn) The method of fabricating a membory according to claim 2, wherein

said step of forming said storage part and said thin-film part includes a step of partially etching said storage material film so that said thin-film part has a thickness of not more than about 95% of the thickness of said storage material film on the average.

4. (Withdrawn) The method of fabricating a memory according to claim 2, wherein

said step of forming said storage part and said thin-film part includes a step of partially etching said storage material film with etching gas containing no chlorine-based gas.

5. (Withdrawn) The method of fabricating a memory according to claim 1, said memory further comprising a memory cell array region formed with said storage material film, a peripheral circuit region and a connecting wire for connecting said memory cell array region and said peripheral circuit region with each other, wherein

said step of patterning said insulator film and said thin-film part of said storage material film includes a step of patterning said insulator film and said thin-film part of said storage material film so that no said thin-film part of said storage material film is present at least in the vicinity of a region connecting said memory cell array region and said connecting wire with each other.

6. (Withdrawn) The method of fabricating a memory according to claim 5, further comprising steps of:

forming an interlayer dielectric film covering at least a portion close to said region connecting said memory cell array region and said connecting wire with each other after patterning said insulator film and said thin-film part of said storage material film, and

forming an opening for connecting said memory cell array region and said connecting wire with each other by etching a prescribed region of said interlayer dielectric film.

7. (Withdrawn) The method of fabricating a memory according to claim 6, further comprising a step of connecting said first electrode film of said memory cell array region and said connecting wire with each other through said opening.

8. (Withdrawn) The method of fabricating a memory according to claim 1, wherein

said step of forming said insulator film includes a step of forming said insulator film having a function of inhibiting hydrogen from diffusion.

9. (Withdrawn) The method of fabricating a memory according to claim 1, wherein

said first electrode film includes a first lower electrode film and a second lower electrode film formed on said first lower electrode film.

10. (Withdrawn) The method of fabricating a memory according to claim 9, wherein

said first lower electrode film has a function of inhibiting oxygen from diffusion.

11. (Withdrawn) The method of fabricating a memory according to claim 1, wherein

said storage material film is either a ferroelectric film or a colossal magnetoresistance film.

12. (Currently Amended) A memory comprising:

a first electrode film which inhibits oxygen diffusion;

a storage material film, formed on said first electrode film, provided with a storage part and a thin-film part having a thickness, smaller than the thickness of said storage part, of at least about 15% of the thickness of said storage part of the average;

a second electrode film formed on aid storage part of said storage material film.

13. (Currently Amended) The memory according to claim 12 wherein said thin-film part has a thickness of not more than about 95% of the thickness of said storage part ~~material film~~ on the average.

14. (Original) The memory according to claim 12, further comprising an insulator film formed to cover said second electrode film and said thin-film part of said storage material film against an etching mask employed for working said thin-film part of said storage material film.

15. (Original) The memory according to claim 14, wherein said insulator film includes a film having a function of inhibiting hydrogen from diffusion.

16. (Currently Amended) A ~~The~~ memory ~~according to claim 12, further~~ comprising:

a first electrode film;

a storage material film, formed on said first electrode film, provided with a storage part and a thin-film part having a thickness, smaller than the thickness of said storage part, of at least about 15% of the thickness of said storage part of the average;

a second electrode film formed on said storage part of said storage material film;

a memory cell array region formed with said storage material film;

a peripheral circuit region; and

a connecting wire for connecting said memory cell array region and said peripheral circuit region with each other, wherein

said storage material film is so patterned that no said thin-film part of said storage material film is present at least in the vicinity of a region connecting said memory cell array region and said connecting wire with each other.

17. (Original) The memory according to claim 16, further comprising an interlayer dielectric film covering at least a portion close to said region connecting said memory cell array region and said connecting wire with each other having an opening, wherein

said first electrode film of said memory cell array region and said connecting wire are connected with each other through said opening.

18. (Original) The memory according to claim 12, wherein said first electrode film includes a first lower electrode film and a second lower electrode film formed on said first lower electrode film.

19. (Currently Amended) A ~~The~~ memory ~~according to claim 18,~~ comprising:

a first electrode film;

a storage material film, formed on said first electrode film, provided with a storage part and a thin-film part having a thickness, smaller than the thickness of said storage part, of at least about 15% of the thickness of said storage part of the average;

a second electrode film formed on said storage part of said storage material film, wherein said first electrode film includes a first lower electrode film and a second lower electrode film formed on said first lower electrode film, and wherein said first lower electrode film has a function of inhibiting oxygen from diffusion.

20. (Original) The memory according to claim 12, wherein said storage material film is either a ferroelectric film or a colossal magnetoresistance film.

21. (Currently Amended) A ~~The~~ memory ~~according to claim 12,~~ comprising:

a first electrode film;

a storage material film, formed on said first electrode film, provided with a storage part and a thin-film part having a thickness, smaller than the thickness of said storage part, of at least about 15% of the thickness of said storage part of the average;

a second electrode film formed on said storage part of said storage material film,

wherein said storage material film is formed to cover the upper surface and the side surfaces of said first electrode film.

22. (Original) The memory according to claim 12, further comprising:

a transistor having pair of source/drain regions, and

a metal plug connected to one of said source/drain regions of said transistor; wherein

said first electrode film is formed to come into contact with said metal plug.